

IN THE CLAIMS

A marked-up version of the claims, showing changes made, may be found in Appendix A, attached hereto. Below is a clean set of all pending claims, submitted under 37 C.F.R. §1.121(c)(3), incorporating any additions, cancellations, and amendments thereto. Please substitute these claims for pending claims of the same number.

1. (Once Amended) A computer system comprising:
- a controller to generate a power state status signal to indicate a power state of a first plurality of components of the computer system; and
 - a voltage regulator to supply a voltage level to the first plurality of components and to increase the voltage level to the first plurality of components when the first plurality of components enters a sleep state, as indicated by the power state status signal.
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2. (Newly Added) The computer system of claim 1, wherein the voltage regulator is to decrease the voltage level to the first plurality of components when the first plurality of components enter a wake state, as indicated by the power state status signal.
3. (Newly Added) The computer system of claim 1, wherein the power state status signal is to further indicate a power state of at least a second component, the voltage regulator to supply the voltage level to the second component and to increase the voltage level to both the second component and to the first plurality

of components when the first plurality of components enters a sleep state and a power state of the second component remains unchanged.


4. (Newly Added) The computer system of claim 3 wherein the power state of the second component that remains unchanged is a sleep state.

5. (Newly Added) The computer system of claim 3, wherein the power state of the second component that remains unchanged is a wake state.



6. (Newly Added) The computer system of claim 3, wherein the voltage regulator is to decrease the voltage level to both the second component and to the first plurality of components when the first plurality of components enters a wake state and a power state of the second component remains unchanged.

7. (Newly Added) The computer system of claim 1, wherein the power state status signal is to further indicate a power state of at least a second component, the voltage regulator to supply the voltage level to the second component and to increase the voltage level to both the second component and to the first plurality of components when the second component enters a sleep state and a power state of the first plurality of components remains unchanged.

8. (Newly Added) The computer system of claim 7, wherein the power state of the first plurality of components that remains unchanged is a sleep state.

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9. (Newly Added) The computer system of claim 7, wherein the power state of the first plurality of components that remains unchanged is a wake state.
10. (Newly Added) The computer system of claim 7, wherein the voltage regulator is to decrease the voltage level to both the second component and to the first plurality of components when the second component enters a wake state and a power state of the first plurality of components remains unchanged.
11. (Newly Added) The computer system of claim 1, further comprising a processor and a hub coupled between the processor and the first plurality of components, the hub being coupled to the voltage regulator and including the controller.
12. (Newly Added) The computer system of claim 1, wherein at least a portion of the controller is distributed among the first plurality of components.
13. (Newly Added) The computer system of claim 1, wherein the power state status signal is an SLP_S3# signal.
14. (Newly Added) The computer system of claim 1, wherein the first plurality of components includes a hard disk drive.
15. (Newly Added) A voltage regulator comprising:
an input to receive a power state status signal to indicate power states of first and second components of a computer system; and

an output to supply a first voltage level to the first and second components during a first period of time and to supply a second voltage level to the first and second components during a second period of time if the power state status signal indicates that the first and second components are in a first power state during the first period of time and the power state status signal indicates that the first and second components are in the first and second power states, respectively, during the second period of time.

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16. (Newly Added) The voltage regulator of claim 15, wherein the first voltage level is lower than the second voltage level, the first power state is a wake state, and the second power state is a sleep state.
17. (Newly Added) The voltage regulator of claim 15, wherein the first voltage level is higher than the second voltage level, the first power state is a sleep state, and the second power state is a wake state.
18. (Newly Added) The voltage regulator of claim 15, wherein the first and second voltage levels are below the nominal voltage level associated with the first and second components.
19. (Newly Added) The voltage regulator of claim 15, further comprising a storage element to store information associated with the power state status signal.

20. (Newly Added) A method comprising:
- generating a power state status signal to indicate a power state of a plurality of components of a computer system;
 - increasing a voltage level supplied to the plurality of components if the power state status signal indicates that a first component of the plurality of components transitions from a wake state to a sleep state; and
 - further increasing the voltage level supplied to the plurality of components if the power state status signal indicates that a second component of the plurality of components transitions from a wake state to a sleep state.
21. (Newly Added) The method of claim 20, further comprising decreasing the voltage level supplied to the plurality of components if the power state status signal indicates that the first component of the plurality of components transitions from a sleep state to a wake state.
22. (Newly Added) The method of claim 20, further comprising decreasing the voltage level supplied to the plurality of components if the power state status signal indicates that a third component of the plurality of components transitions from a sleep state to a wake state.
23. (Newly Added) The method of claim 20, wherein generating a power state status signal includes generating a SLP_S3# signal.